MEG-03-002

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June 14, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/802,566 03/17/04

M.S. Lin

A HIGH PERFORMANCE IC CHIP HAVING DISCRETE DECOUPLING CAPACITORS ATTACHED TO ITS IC SURFACE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 21, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 6/21/04

U.S. Patent Application MEG-02-014, Serial No. 10/855,086, filed 05/27/04, "A Wafer Level Processing Method and Structure to Manufacture Two Kinds of Bumps, Gold and Solder, On One Wafer," discusses a wafer structure and fabrication method to form both gold and solder bumps on the same wafer.

The following two U.S. Patents teach methods and structures of mounting a discrete component on the surface of an IC chip:

1) U.S. Patent 6,303,423 to Lin, "Method for Forming High Performance System-on-Chip Using Post Passivation Process."

2) U.S. Patent 6,515,369 to Lin, "High Performance System-on-Chip Using Post Passivation Process."

The following two U.S. Patents discloses a post-passivation interconnection process:

1) U.S. Patent 6,495,442 to Lin et al., "Post Passivation Interconnection Schemes on Top of the IC Chips."

2) U.S. Patent 6,383,916 to Lin, "Top Layers of Metal for High Performance IC's."

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The following two U.S. Patents discloses an integrated circuit lead frame with capacitors formed on the lead frame and bonded to the bottom surface of the chip for decoupling purposes:

1) U.S. Patent 6,184,574 to Bissey, "Multi-Capacitance Lead Frame Decoupling Device."

2) U.S. Patent 6,504,236 to Bissey, "Semiconductor Die Assembly Having Leadframe Decoupling Characters and Method."

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
MEG-03-002	10/802,566
Applicant: M.S. Lin	
Filing Date: 03/17/04	Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6303423	10/16/01	Lin	438	238	11/27/00
	6515369	2/4/03	Lin	257	773	5/28/02
	6495442	12/17/02	Lin et al.	438	618	10/18/00
	6383916	5/7/02	Lin	438	637	2/17/99
	6184574	2/6/01	Bissey	257	666	10/12/99
	6504236	1/7/03	Bissey	257	666	8/24/01

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

Co-pending U.S. Patent MEG-02-014, filed 05/27/04, Serial # 10/855,086, assigned to the same assignee.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.